DECLARATION

In the matter of
U.S.Serial No. 09/941,683
in the name of Ren UCHIDA

I, the undersigned, Kazuteru SHIMURA, of Fujimoto Patent and Law Office, of Room 317, Sanno Grand Building, 14-2, Nagata-cho 2-chome, Chiyoda-ku, Tokyo, Japan, do solemnly and sincerely declare as follows:

1. That I am well acquainted with the English and Japanese languages and am competent to translate Japanese into English and vice versa.

2. That I have executed, with the best of my ability, a true and correct translation to the attached copy of the complete description, claims, drawings and abstract originally filed as Japanese Patent Application No. 2000-299844.

This fourth day of August, 2003

Kazuteru SHIMURA

(Translation)

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This is to certify that the annexed is a true copy of the following application as filed with this Office.

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[TITLE OF THE INVENTION]

TESTING METHOD AND TESTING DEVICE FOR SEMICONDUCTOR INTEGRATED CIRCUITS

[SCOPE OF CLAIM FOR PATENT]

[CLAIM 1]

A testing method for testing a semiconductor integrated circuit incorporating a plurality of DA converters and a reference voltage generating circuit for determining gradation output voltage characteristics, using a semiconductor testing device having a comparison circuit for making a judgement by comparing the gradation output voltage with a reference voltage,

characterized in that a section of gradation levels to be tested is determined by setting different potentials at reference power supply input terminals of the reference voltage generating circuit so that the semiconductor testing device applies the voltage between the reference power source input terminals, and the input gradation data signals for the gradation levels within the section are made in correspondence with gradation output voltages, whereby the test of the gradation output voltages are digitally judged by the semiconductor testing device.

[CLAIM 2]

A testing method for a semiconductor integrated circuit

according to Claim 1, wherein the reference voltage generating circuit increases or decreases the potential difference between adjacent gradation outputs at the analog voltage outputs, in conformity with the voltage applied between the reference power supply input terminals from the semiconductor testing device.

[CLAIM 3]

A testing method for a semiconductor integrated circuit according to Claim 1, wherein, by assigning correspondence between the voltage settings provided from the semiconductor testing device and the input data, the DA converters and the reference voltage generating circuit selectively test the output levels of the analog voltage outputs.

[CLAIM 4]

A testing method for a semiconductor integrated circuit according to Claim 1, wherein the mutual relationship between the input data corresponding to each output voltage level, calculation of the expected output voltage in the semiconductor integrated circuit specification and setting of the expected output voltage levels, the voltage judgement value levels of comparison judgement circuit for judgement of the output voltages, and the change of the set test number with time, are all handled based on address or variable management, so as to be able to verify the reliability of the test accuracy.

[CLAIM 5]

A testing device for testing a semiconductor integrated circuit incorporating a plurality of DA converters and a reference voltage generating circuit for determining gradation output voltage characteristics, using a comparison judgement circuit for making a judgement by comparing the gradation output voltage with a reference voltage, characterized in that different voltages are output to the reference power supply input terminals at one end and at the other end of the section of gradation levels to be tested in the semiconductor integrated circuit.

[CLAIM 6]

A testing device for a semiconductor integrated circuit according to Claim 5, wherein the voltages are output to two or more reference power supply input terminals at least including the reference power supply input terminal at one end of the section of gradation levels to be tested in the semiconductor integrated circuit.

[CLAIM 7]

A testing device for a semiconductor integrated circuit according to Claim 5, wherein a reference power supply input terminal that is not connected to the semiconductor testing device is present within the section of gradation levels to be tested in the semiconductor integrated circuit.

[CLAIM 8]

A testing device for a semiconductor integrated circuit according to Claim 5, wherein two or more sections of gradation levels to be tested are present in the semiconductor integrated circuit.

[DETAILED DESCRIPTION OF THE INVENTION]

[0001]

[Technical Field of the Invention]

The present invention relates to a method of testing a semiconductor integrated circuit having the function of outputting a plurality of gray scale levels (to be referred to hereinbelow as 'gradation levels') and a plurality of DA converters (to be referred to hereinbelow as 'DACs') as to its gradation output voltages as well as relating to a testing device therefor. In particular, the present invention relates to a testing method and testing device for semiconductor integrated circuits wherein the gradation output voltage output from each DAC can be tested in a short time and with high precision. Here, the gray scale level means the output voltage level that determines the brightness level of dot representation in a liquid crystal panel and the like.

[0002]

[Prior Art]

With the trend of liquid crystal panels toward high definition, the LCD driver LSIs provided on liquid crystal panels tend to develop into multi-output and multi-gradation

configurations. An LCD driver LSI has a 'Gamma correction resistance circuit' or a 'Gamma correction capacitor circuit' as a reference voltage generating circuit incorporated inside the device. Voltage is applied to this reference voltage generating circuit via reference power supply input terminals. The number of gradation levels of an LCD driver LSI is determined by the division ratio (resistance division ratio in the case of a Gamma correction resistance circuit, and capacitance division ratio in the case of a Gamma correction capacitor circuit) to this applied voltage. The more minutely refined this division ratio is, the more gradation levels is included.

[0003]

In addition, to achieve multi-gradation display, the LCD driver has built-in DACs (which convert digital input image data into analog gradation output voltages) corresponding to the number of gradation levels and outputs the gradation voltages. For example, an LCD driver for 64 gradation display use has 6 bit built-in DACs, an LCD driver for 256 gradation display use has 8 bit built-in DACs, and an LCD driver for 1024 gradation display use has 10 bit built-in DACs.

[0004]

In the test for a multi-gradation, multi-output LCD driver, whether all the gradation voltage values output from each DAC present the correct voltage values corresponding

to respective levels of digital image data, and whether the gradation voltages output from different DACs are equal to each other, are tested.

[0005]

A conventional test method will be described taking an example of an LCD driver with built-in DACs of m outputs and n gradation levels.

Fig.7 shows a schematic circuit diagram of a conventional semiconductor testing device including an LCD driver and a high accuracy voltage measurement device.

From a semiconductor test device (to be referred to hereinbelow as 'tester') 60 to the LCD driver 51, predetermined gradation digital data for all the output terminals, for each gradation level, is sequentially input to the reference power supply voltage input terminals 6-1 to 6-x. In a reference voltage generating circuit 8, reference voltages are generated. The digital data of each gradation level is DA converted (a reference voltage corresponding to the gradation data is selected) by built-in DAC circuit 2-1 to 2-m in the device. The converted signals are processed through the output amplifiers so that analog voltages are output from output terminals 3-1 to 3-m as gradation output voltages.

[0006]

The analog voltages output from LCD driver 51 are input into tester channels 11-1 to 11-m that are input terminals

of tester 60. Using a high accuracy voltmeter 62 built in tester 60, the analog outputs 1 up to the m-th output are sequentially measured, level by level. The measurements are stored successively into a built-in memory 63 incorporated in tester 60.

[0007]

This procedure is repeated for the n gradations, and finally the data for all outputs, all gradations are stored in memory 63. As a result, m × n pieces of voltage data are stored. All the voltage data stored in memory 63 are used for calculation by a built-in computational device 64 in tester 60. In this way, all the gradation voltage values (indicating 'the deviation to maximum and deviation to minimum of the gradation output voltages from ideal gradation output voltage values', which will be referred to hereinbelow) for every output, and the uniformity of the gradation voltage values over all the outputs (indicating 'inter-terminal fluctuation', which will be referred to hereinbelow), can be determined by calculation.

[0008]

General criteria for gradation voltage values are of three factors, i.e., the deviation to maximum and deviation to minimum of gradation output voltages output from all the output terminals 3-1 to 3-m, with respect to the ideal gradation output voltage for each gradation level, and inter-terminal

fluctuation. Here, since the judgement values for deviation to maximum and deviation to minimum of the gradation output voltage from the ideal gradation output voltage value should be ±30 [mV] and the inter-terminal fluctuation should be about 35 [mV], to pick out defective products, a very high measurement accuracy is needed.

[0009]

Though the existing testing method of gradation output voltages has been described heretofore, the test items of an LCD driver should include, other than the test for gradation output voltages, input leak, Gamma correction resistance, function operations, high-frequency clock operation and current consumption. However, in the test execution time for all the test items, 70-80% is taken up by the test for gradation output voltages.

[0010]

Other than high-accuracy voltage meters, a comparison judgement circuit (hereinafter 'comparator') is used as a judgement module provided in the tester.

Fig.8 is a schematic circuit diagram showing a conventional semiconductor testing device made of an LCD driver and comparators. Here, the gradation output voltages output from LCD driver 51 are checked by built-in comparators 12-1 to 12-m in tester 70.

[0011]

Similarly to the conventional tester 60 based on a high-accuracy voltage meter, the pre-set gradation digital data for all the output terminals are sequentially input for every gradation level from tester 70 to the LCD driver 51. The gradation digital data of each level is DA converted (a reference voltage corresponding to the gradation data is selected) by the built-in DAC circuits 2-1 to 2-m in the device. The signals are processed through output amplifiers so that analog voltages are output from output terminals 3-1 to 3-m as gradation output voltages. These analog voltages are input into comparators 12-1 to 12-m of tester 70, to carry out judgement based on the comparison judgement voltage level values corresponding to the predetermined gradation digital data for all the output terminals.

[0012]

Fig.9 is a correlation diagram of the set voltages of the judgement reference levels and the gradation output voltages at the time of comparator judgement.

The comparison judgement voltage level indicates two voltage values that determine the upper limit and lower limit of the gradation output voltage for each level. In this chart, the voltage region between the upper and lower limits is judged to be PASS, and the regions above the upper limit and below the lower limit are shown to be judged to be FAIL. However, depending on the test contents (the setting of expectation

values), the opposite setting is also possible.

[0013]

An LCD driver that can be tested using a testing device with comparators has been disclosed in Japanese Patent Application Laid-open 2000-165244. Fig.10 shows a circuit diagram showing this LCD driver.

In an LCD driver LSI 81 shown in Fig.10, gradation data is given to a bus line 83 of the DAC through a decoder 82. For each gradation data, one of the gradation voltage selection switches 85, which each select one output voltage from the reference power supply terminals 6-1 to 6-10 and the resistance divider circuit 13, is selected, so as to output a gradation voltage through an output amplifier 84 from each of output terminals 3-1 to 3-m.

[0014]

A circuit of relays 85 and 86 is serially connected between adjacent reference power supply terminals 6-1 to 6-10 while the connection point of the relays 85 and 86 is connected to the mid-point of resistance divider circuit 13.

Applied to the reference power supply terminal at one end is a power supply voltage (5V) while the reference power supply terminal at the other end is applied with the ground voltage (0V). Now, when testing the upper part, relay 85 is turned OFF, and relay 86 is turned ON. As a result, a voltage of 5V is applied between both ends of the upper part of

resistance divider circuit 13.

[0015]

Next, the specified gradation data is applied to decoder 82 to make it output analog voltages. At this time, the potential difference between output voltages is 5V/4=1.25, a rather great value. That is, the first gradation voltage is 5 V, the second gradation voltage is 3.75 V, the third gradation voltage is 2.50 V, the fourth gradation voltage is 1.25 V and the fifth gradation voltage is 0 V. Thus, if the comparator has an accuracy of 0.5V or lower for example, the voltage of every gradation can be recognized, so that digital judgement using a comparator is possible. When testing the lower part, the first relay 85 is turned ON, and the relay 86 is turned OFF.

[0016]

[Problems to be Solved by the Invention]

The problems of conventional semiconductor testing equipment are summarized as follows.

[0017]

(1) The problem of the test using a high accuracy voltage measurement equipment

With the trend towards multi-output and multi-gradation of LCD drivers, the semiconductor circuit test using high-accuracy voltage measurement equipment shown in Fig.7 needs to effect sequential procedures of output judgement

of the device, hence the time required for the gradation output voltage test sharply escalates due to increase in the amount of data to be read and increase in data processing time. Further, since it is necessary to measure more accurately the gradation output voltage values, an expensive tester mounted with a plurality of high-accuracy voltage meters is required.

[0018]

Furthermore, test accuracy becomes more difficult to ensure with the advance of multi-gradation. That is, with the advance of multi-gradation, the output potential difference between gradation levels are greatly decreased. This is determined by the aforementioned, Gamma correction resistance circuit incorporated inside the device as a reference voltage generating circuit, based on the resistance division ratio with respect to the voltage applied through the reference power supply input terminals. The more minutely divided this division ratio is, the more advanced the multi-gradation is. That is, by simple calculation, the output gradation potential difference between neighboring gradations of a 6 [V] driven LCD driver of 64 gradations is 93.75 [mV] (6000 [mV]/64 gradations). By contrast, the output potential difference of a 6 [V] driven LCD driver of 256 gradations is 23.44 [mV] (6000 [mV]/256 gradations). As a result, when the output potential difference between

neighboring gradation levels is smaller than the output voltage deviation (inter-terminal fluctuation), it is difficult for the judgement values to ensure the test accuracy for checking that the output voltage of each gradation level corresponds to the input image digital data even with a high-accuracy voltage meter because level shift by one gradation, etc., may occur due to improper reading of data. Moreover, a strict setting of the judgement values for the test of inter-terminal fluctuation is difficult because of the specification of the LCD drivers, as understood from the aforementioned example of the inter-terminal fluctuation being 35 [mV].

[0019]

(2) The problem of the test using comparators

The advantage of the semiconductor circuit test using the comparators shown in Fig.8 is that all the outputs from the device can be judged altogether in parallel, greatly reducing the testing time. As comparators are relatively inexpensive, a plurality of comparators, equal to the number of LSI outputs are mounted in a tester.

However, as shown in Fig.9, as to the accuracy of a comparator, it is impossible to distinguish a gradation output voltage level difference equal to or lower than about 100 [mV]. When a plurality of gradation levels exist within the minimum width of the comparison judgement voltage level

(reference voltage ±100 [mV]), the target gradation level to be tested becomes unclear. In addition, it is impossible to determine the accurate values of the deviation to maximum and deviation to minimum of each gradation output voltage level and the inter-terminal fluctuation over the outputs. Therefore, differentiation of a gradation output voltage level difference less than about 0.1 [V] is not possible, and it is difficult to ensure the test accuracy as to functional operation precision of the LCD driver. Hence, in general, existing comparator judgement is not used in the gradation output voltage test for LCD drivers, and is used only for the test items which are not related to the accuracy of gradation output voltages of LCD drivers.

[0020]

For instance, when an LCD driver outputs 3.0 [V] for a certain gradation level, the upper judgement limit of this gradation level by the comparator judgement is 3.1 [V] maximum while the lower limit by the judgement is 2.9 [V] minimum, because of the comparator accuracy. That is, the potential difference between these two judgement levels is 0.2 [V]. For the 6 [V] driven LCD driver of 256 gradations shown in the foregoing example, 8 to 9 gradation output levels are included between these two judgement levels since the gradation output potential difference per gradation is 23.44 [mV]. Hence, it is impossible to check each gradation output

voltage corresponding to the input data of a single gradation level.

[0021]

Furthermore, Fig.11 is a schematic diagram showing a conventional example of applying reference power supply voltages.

For instance, when a 10 [V] driven LCD driver 1 of 256 gradations has 6 reference power supply input terminals, from the high voltage of the gradation output voltages, V1=10 [V], V2=8 [V], V3=6 [V], V4=4 [V], V5=2 [V], V6=0 [V] are applied. The gradation output voltage levels between the reference power supply input terminals is generated by dividing the potential difference, 2 [V] into the output voltage for each gradation level, based on the division ratio according to the Gamma correction resistance characteristics. Accordingly, if the number of gradation output voltage levels to be created across the potential difference of 2 [V] between the adjacent reference power supply input terminals, is 51 gradations (256 gradations divided into 5 sections, for each of the reference power supply input terminals), the gradation output voltage potential difference for each gradation is about 40 [mV]. When comparator judgement is made, it is impossible to discriminate a gradation output voltage level difference equal to or lower than about 100 [mV], as shown in Fig.9. Since about 5 gradation levels (calculated from

the comparator judgement width of 200 [mV]/the potential difference per gradation, about 40 [mV]), exist within the minimum width (reference voltage ±100 [mV]) of the comparison judgement voltage level, the gradation levels to be tested become unclear.

[0022]

An LCD driver that can differentiate gradation output voltage level difference using comparators has been disclosed in Japanese Patent Application Laid-open 2000-165244. This LCD driver, however, needs an extra relay circuits, and hence needs an enlarged chip area. In view of device design, provision of a relay circuit presenting an ON resistance of 1 KΩ when it is switched on between adjacent reference power supply terminals increases the chip area by about 7%. To lower the ON resistance of the switch, it is necessary to further increase the relay circuit area, which leads further increase of the chip area.

[0023]

The voltage applied to resistance division circuit 13 for the gradation output levels to be tested should be doubled in theory when one side of the relay circuit is short-circuited. However, actually, it could not be doubled because of the ON resistance of the relay circuit. The reason for this is that as the resistance division circuit (Gamma correction resistance) moves towards a low resistance configuration,

the ON resistance of the relay circuit increases relatively. Consequently, the voltage drop due to the ON resistance increases, and the voltage is not increased as much as expected.

[0024]

Furthermore, in the trend towards diversified device functions, when an existing tester (having fewer tester channels) is used for testing, the channels to control the relays become necessary, and testing plan becomes complicated.

[0025]

The object of the present invention is to provide a testing method for semiconductor integrated circuits and a testing device therefor, which realizes sharp reduction in testing time and high-accuracy testing regardless of the measurement accuracy of the judgement module by controlling the gradation voltage levels output from DA converters, based on the setting of the reference power supply voltages applied to the reference voltage generating circuit, in the test of LCD drivers which tend to develop into multi-output and multi-gradation configurations.

[0026]

[Means for Solving the Problems]

The present invention is a testing method for testing a semiconductor integrated circuit incorporating a plurality of DA converters and a reference voltage generating circuit

for determining gradation output voltage characteristics, using a semiconductor testing device having a comparison circuit for making a judgement by comparing the gradation output voltage with a reference voltage.

The method is characterized in that a section of gradation levels to be tested is determined by setting different potentials at reference power supply input terminals of the reference voltage generating circuit so that the semiconductor testing device applies the voltage between the reference power source input terminals, and the input gradation data signals for the gradation levels within the section are made in correspondence with gradation output voltages, whereby the test of the gradation output voltages are digitally judged by the semiconductor testing device.

[0027]

The present invention is also a testing method for a semiconductor integrated circuit wherein the reference voltage generating circuit increases or decreases the potential difference between adjacent gradation outputs at the analog voltage outputs, in conformity with the voltage applied between the reference power supply input terminals from the semiconductor testing device.

[0028]

The present invention is a testing method for a semiconductor integrated circuit, wherein, by assigning

correspondence between the voltage settings provided from the semiconductor testing device and the input data, the DA converters and the reference voltage generating circuit selectively test the output levels of the analog voltage outputs.

[0029]

The present invention is a testing method for a semiconductor integrated circuit, wherein the mutual relationship between the input data corresponding to each output voltage level, calculation of the expected output voltage in the semiconductor integrated circuit specification and setting of the expected output voltage levels, the voltage judgement value levels of comparison judgement circuit for judgement of the output voltages, and the change of the set test number with time, are all handled based on address or variable management, so as to be able to verify the reliability of the test accuracy.

[0030]

The present invention is a testing device for testing a semiconductor integrated circuit incorporating a plurality of DA converters and a reference voltage generating circuit for determining gradation output voltage characteristics, using a comparison circuit for making a judgment by comparing the gradation output voltage with a reference voltage.

The device is characterized in that different voltages

are output to the reference power supply input terminals at one end and at the other end of the section of gradation levels to be tested in the semiconductor integrated circuit.

[0031]

The present invention is a testing device for a semiconductor integrated circuit, wherein the voltages are output to two or more reference power supply input terminals at least including the reference power supply input terminal at one end of the section of gradation levels to be tested in the semiconductor integrated circuit.

[0032]

The present invention is a testing device for a semiconductor integrated circuit, wherein a reference power supply input terminal that is not connected to the semiconductor testing device is present within the section of gradation levels to be tested in the semiconductor integrated circuit.

[0033]

The present invention is a testing device for a semiconductor integrated circuit, wherein two or more sections of gradation levels to be tested are present in the semiconductor integrated circuit.

[0034]

In the present invention, for all the gradation levels during test each gradation output voltage is set apart by

the output voltage variance of the LCD driver or greater from the adjacent gradation potentials. In addition, even for comparators having relatively low judgement accuracy, it is possible to achieve tests focused on individual gradation output voltages corresponding to input data of single gradation levels. Therefore, it is possible to carry out separate tests that can easily detect data corruption, etc., inside the DACs, for each gradation level to be tested. Consequently, it is possible to ensure high test accuracy, regardless of the accuracy of the measurement and testing equipment.

Furthermore, because it is possible to digitally judge all the outputs at the same time by the testing device using comparator circuits, high-accuracy measurement can be achieved by a conventional, inexpensive tester, in a sharply reduced test period.

[0035]

[Embodiment of the Invention]

The embodiment of the present invention will be described hereinbelow with reference to the drawings.

Fig.1 is a schematic diagram of an example of applying reference power supply voltages to an LCD driver with a reference power supply generating circuit of a Gamma correction resistance type.

An LCD driver 1 comprises six reference power supply

input terminals V1 to V6, a reference voltage generating circuit 8 made of a Gamma correction resistance 13 and DA converters 2-1 to 2-m, so as to generate m levels of gradation voltages. Accordingly, the basic structure is the same as the LCD driver 1 of Fig.11, and is a 10 [V] driven LCD driver for 256 gradations, and forms the same device model as the configuration having six reference power supply input terminals.

[0036]

Moreover, arranged in the prior stage of liquid crystal driver 1 is a tester power supply 7, which supplies voltage to reference power supply input terminals V1 to V6. The tester as the testing device of this liquid crystal driver 1, though not illustrated, has the same structure as the tester 70 in Fig.8, and judges the gradation output voltages, output from liquid crystal driver 1 by a comparison judgement circuit or comparators.

In Fig.1A the DA converters corresponding to the levels between the reference power supply terminals V1 and V2 are the test targets and in Fig.1B the DA converters corresponding to the levels between the reference power supply terminals V2 and V3 are the test targets.

[0037]

As shown in Fig.1A, two voltages, 10 [V] and 0 [V] (the upper limit and lower limit of drive voltage specification

of the LCD driver) are assigned as the set values of the reference power supply voltages. That is, the reference power supply voltages are set so that V1=10[V], V2=0[V], V3=0[V], V4=0[V], V5=0[V] and V6=0[V]. A reference power supply potential difference of 10 [V] is created between the reference power supply terminals V1 and V2. Testing the gradation levels included between the reference power supply terminals V1 and V2 makes it possible to create a potential difference of about 200 [mV] (potential difference between the reference power supply terminals, 10000 [mV]/51 gradation levels) between adjacent output gradation levels.

[0038]

Accordingly, as in the diagram shown in Fig.2 for depicting the correlation between the set judgement reference levels and the gradation output voltage during the operation in which the reference power supply voltages are set, it is possible to set up a comparator judgement range for every gradation output voltage level. Hence it is possible to achieve tests focused on individual gradation output voltages corresponding to input data of single gradation levels.

The gradation levels included between the reference power supply terminals are tested while the input data and the setting of the comparator judgement range are sequentially switched for every gradation level, thus all the gradation levels included in that section are tested.

[0039]

Subsequently, when the gradation output voltage levels included between the reference power supply terminals V2 and V3 are tested, the input settings of the power supply applied to the reference power supply terminals are changed again as shown in Fig.1B: the reference power supply voltages are set so that V1=10 [V], V2=10 [V], V3=0 [V], V4=0 [V], V5=0 [V] and V6=0 [V], and all the gradation levels included in that section are tested in a similar manner. Similarly, every gradation output voltage level is tested while sequentially changing the settings of the reference power supply voltage, whereby it is possible to achieve tests focused on individual gradation output voltages corresponding to the input data of single gradation levels for all the gradation output voltage levels, included in the LCD driver.

Here, the foregoing reference power supply voltages applied to the reference power supply input terminals are not limited to two values, in some cases depending on the judgement accuracy of the measurement and judgement equipment. The detail of this will be described later.

[0040]

Accordingly, with this testing technique, the gradation output voltages for all the gradation levels during test are set apart by the output voltage variance (fluctuation) of the LCD driver or greater from the adjacent gradation

potentials. In addition, even for comparators having relatively low judgement accuracy, it is possible to achieve tests focused on individual gradation output voltages corresponding to input data of single gradation levels. This makes it possible to carry out separate tests that can easily detect data corruption, etc., inside the DACs, for each gradation level to be tested. Consequently, it is possible to ensure high test accuracy, regardless of the accuracy of the measurement and testing equipment.

[0041]

Further, since digital judgement on all the outputs at the same time can be made by an inexpensive testing modules made of comparator circuits, etc., (a plurality of modules, equal to the number for all the outputs of the LSI, are mounted on the semiconductor testing device because they are inexpensive), it is possible to achieve high-accuracy measurement in a sharply reduced test period, using a conventional, inexpensive tester.

[0042]

Fig.3 and Fig.4 show examples of set voltages that are applied from the tester power supply to the reference power supply input terminals of the LCD driver, in the embodiment of the present invention. For the testing method according to the present invention, the basic principle of the testing method is as follows. Specifically, similar to the foregoing

description, the input voltages applied to the several reference power supply input terminals in the semiconductor integrated circuit are set so that the potential difference for the gradation output voltage levels included between the reference power supply input terminals to be tested only are set to expand while the potential difference for the gradation output voltage levels included between the reference power supply input terminals which are not the test target are set to be low. Now, its application examples will be described.

[0043]

Fig.3 is a schematic diagram showing setting examples of applying reference power supply voltages to an LCD driver with a reference power supply generating circuit of a Gamma correction resistance type.

In Fig.3A the DA converters corresponding to the levels between the reference power supply terminals V1 and V3 are to be tested, and in Fig.3B the DA converters corresponding to the levels between the reference power supply terminals V3 and V5 are to be tested.

[0044]

Fig.3 shows the same device model as a 20 [V] driven LCD driver of 256 gradations, having six reference power supply input terminals.

As shown in Fig.3A, when the reference power supply voltages are set so that V1=20[V], V2=open, V3=0[V], V4=0[V],

V5=0[V] and V6=0[V], a reference power supply potential difference of 20 [V] can be produced between the reference power supply terminals V1 and V3. Testing the gradation levels included between the reference power supply terminals V1 and V3 makes it possible to create a potential difference of about 200 [mV] (potential difference between the reference power supply terminals, 20000 [mV]/102 gradation levels) between adjacent output levels of gradation.

[0045]

Accordingly, as in the diagram shown in Fig.2 for depicting the correlation between the set judgement reference levels and the gradation output voltage during the operation in which the reference power supply voltages are set, it is possible to set up a comparator judgement range for every gradation output voltage level. Hence it is possible to achieve tests focused on individual gradation output voltages corresponding to input data of single gradation levels.

[0046]

The gradation levels included between the reference power supply terminals are tested while the input data and the setting of the comparator judgement ranges are sequentially switched, thus all the gradation levels included in that section are tested.

[0047]

Subsequently, when the gradation output voltage levels

included between the reference power supply terminals V3 and V5 are to be tested, the input settings of the power supply applied to the reference power supply terminals are changed again as shown in Fig.3B: the reference power supply voltages are set so that V1=20 [V], V2=20 [V], V3=20 [V], V4= open, V5=0 [V] and V6=0 [V], and all the gradation levels included in that section are tested in the same manner. Similarly, every gradation output voltage level is tested while sequentially changing the settings of the reference power supply voltage, whereby it is possible to achieve tests focused on individual gradation output voltages corresponding to input data of single gradation levels for all the gradation output voltage levels, included in the LCD driver.

[0048]

Further, in the examples of setting the reference power supply voltages up to here, two voltages (the upper limit and lower limit of the drive voltage specification of the LCD driver) are assigned as the set values of the reference power supply voltages. However, depending on the number of levels of gradation included between the reference power source terminals and the drive voltage of the LCD driver, a test can also be achieved with the reference power source set as follows.

[0049]

Fig.4 is a schematic diagram showing setting examples

of applying reference power supply voltages to an LCD driver with a reference power supply generating circuit of a Gamma correction resistance type.

In Fig.4A, the DA converters corresponding to the levels between the reference power supply terminals V1 and V2, the levels between terminals V3 and V4 and the levels between terminals V5 and V6 are to be tested. In Fig.4B, the DA converters corresponding to the levels between the reference power supply terminals V2 and V3 and the levels between terminals V4 and V5 are to be tested. In this case, it is also possible to execute the DA converters corresponding to the levels between terminals V3 and V4. However, the test has already completed at the setting stage of the reference power supply voltages shown in Fig.4A, hence there is no need for the test as it is redundant.

[0050]

Fig.4 shows the same device model as a 6 [V] driven LCD driver of 64 gradations, having six reference power supply input terminals.

As shown in Fig.4A, when the reference power supply voltages are set so that V1=6[V], V2=4[V], V3=4[V], V4=2[V], V5=2[V] and V6=0[V], a reference power supply potential difference of 2 [V] can be produced between the reference power supply terminals V1 and V2, between V3 and V4 and between V5 and V6. Testing the gradation levels included between the

reference power supply terminals V1 and V2, between V3 and V4 and between V5 and V6 makes it possible to create a potential difference of about 154 [mV] (potential difference between the reference power supply terminals, 2000 [mV]/13 gradation levels) between adjacent output levels of gradation (the number of gradation levels, 13 is calculated from 64 gradation/5, the number of reference voltage sections). Accordingly, as in the diagram shown in Fig.2 for depicting the correlation between the set judgement reference levels and the gradation output voltage during the operation in which the reference power supply voltages are set, it is possible to set up a comparator judgement range for every gradation output voltage level. Hence it is possible to achieve tests focused on individual gradation output voltages corresponding to input data of single gradation levels.

[0051]

The gradation levels included between the reference power supply terminals are tested while the input data and the setting of the comparator judgement range are sequentially switched, thus all the gradation levels included in that section are tested.

[0052]

Subsequently, when the gradation output voltage levels included between the reference power supply terminals V2 and V3 and between V4 and V5 are to be tested, the input settings

of the power supply applied to the reference power supply terminals are changed again as shown in Fig.4B: the reference power supply voltages are set so that V1=6 [V], V2=6 [V], V3=4 [V], V4=2 [V], V5=0 [V] and V6=0 [V], and all the gradation levels included in that section are tested in the same manner. As a result, it is possible to achieve tests focused on individual gradation output voltages corresponding to input data of single gradation levels for all the gradation output voltage levels, included in the LCD driver.

[0053]

Thus, testing each of the gradation output voltage levels included between the several reference power supply input terminals of the semiconductor integrated circuit makes it possible to achieve high-accuracy tests in a sharply reduced test period regardless of the measurement accuracy of the judgement module. At this time, the potential difference for the gradation output voltage levels included between the several reference power supply input terminals only are set to expand while the potential difference for the gradation output voltages included between the reference power supply input terminals which are not the test target are set to be low. This status of settings is the dedicated test mode of the tester.

[0054]

From the above, with the testing method according to

the present invention, it is possible to configure various kinds of reference power supply voltage settings, depending on the mutual relationship between the number of gradation levels included between the reference power supply terminals, the drive voltage of the LCD driver and the number of reference power supply terminals of the LCD driver. That is, it is possible to increase the flexibility of the setting manner of the reference power supply voltages by taking into account the testing specification of the present invention in the design stage of the LCD driver and by reflecting their mutual relationship. The smaller the number of the gradation levels included between the reference power supply terminals, the higher the degree of flexibility of reference power supply voltage setting. In order to deal with the development of LCD drivers into multi-gradation, the number of reference power supply terminals may be increased. As for the drive voltage of LCD drivers, since the higher the specified drive voltage is, the more types of methods of assigning the voltages over the reference power supply terminals can be taken, it is possible to increase the flexibility of the settings of the reference power supply voltages.

[0055]

Here, the technique of setting the reference power supply voltages according to the present invention can provide the same effect with regards to ensuring test accuracy, even in

a test where high-accuracy voltmeters are used.

[0056]

Next, description will be made on the characteristics relating to a test program that achieves high testing accuracy in a short time regardless of the accuracy of the measurement and testing equipment, at the time of comparator judgement by the present invention as well as the embodiment of a fail check technique that enables easy verification of one-bit accuracy warranty.

[0057]

To begin with, the flow of the setting with regards to the gradation output voltage test based on the reference power supply voltage setting technique of the present invention, for performing the test of every gradation output voltage by comparator judgement will be described together with its problems.

Fig.5 shows a flowchart showing the steps required when conventional gradation output voltages are tested based on comparator judgement.

[0058]

First, at Step S11, the power supply for driving the LCD driver and the reference power supply according to the aforementioned reference power supply voltage setting technique are activated. Then, at Step S12, selection of an input data pattern program is made. Here, the input data

pattern means image data (of gray scale levels corresponding to RGB output) that determines gradation output voltages output from the LCD driver. For the function tests other than the usual gradation output voltage test, one data pattern program is used for one gradation level test. Accordingly, when the test for gradation output voltages is performed based on comparator judgement, as many data pattern programs as the number of all the gradations are needed in order to test all the gradation output voltage levels. Since the number of pattern programs that can be set in a semiconductor testing device is limited, the gradation output voltage test is difficult to achieve based on comparator judgement.

[0059]

Next, the judgement range necessary for comparator judgement and the expected gradation output voltage level are set. This provides the setting of the upper limit level and lower limit level for the gradation output voltage to be tested, whereby the test is implemented so that each gradation output voltage level will fall in the range therebetween. This method is feasible because the potential differences from the neighboring upper and lower gradation voltage levels are great. Here, the voltage values for the upper limit level and the lower limit level should be set taking into consideration the set conditions of the reference power supply. For example, when 20 gradation levels exist

between the reference power supply terminals to be tested and if a potential difference of 4 [V] is applied from the reference power supply between the reference power supply terminals, the potential difference between neighboring gradation outputs results in 4000 [mV]/20 gradations = 200 [mV/gradation]. The comparator judgement range is set to be ±(200 [mV] - 30 [mV]), taking into account the inter-terminal fluctuation voltage (30 [mV], assumed here) due to the output voltage characteristics of the LCD driver and that the values will not overlap the neighboring gradation output voltage ranges.

However, as the voltage recognition accuracy of comparators is about ±100 [mV], the permissible values of the comparator's acceptance range should fall within ±100 [mV] to ±170 [mV].

[0060]

Since the permissible value of the comparator judgement range determines the test accuracy, the optimal comparator judgement range voltage should be set based on the fail check technique described later. Further, since, with regards to the LCD driver specification, the gradation output voltage levels between the reference power supply input terminals depend on the Gamma correction resistance characteristics, this corresponds to unequal division.

[0061]

The setting of the expected gradation output voltage includes setting of the gradation output voltage level of the relevant test gradation calculated from the set reference power supply voltage values (calculated by the formula for the ideal value of the gradation output voltage in the LCD driver specification) and the upper limit and lower limit calculated from the determined comparator judgement range.

[0062]

Finally, a test gradation number is assigned to the gradation output voltage level to be tested. At Step S13, the data pattern program set beforehand is implemented so as to make judgement. The foregoing steps for test setting, Step S S12 and S13, are repeated the number of times equal to the number of the gradation output voltage levels of the LCD driver to be tested, whereby all the gradation output voltage levels are tested. Accordingly, the test program for testing all gradation output voltage levels becomes very long, and the time for the optimization of the permissible values of the comparator judgement range and for debug and revision of the test program, etc., becomes huge.

[0063]

Next, the features relating to the data pattern program and the test program for solving the problems of the aforementioned test setting flow will be described in detail.

Fig.6 is a flowchart of a test which, based on the reference

power supply voltage setting technique according to the present invention, enables optimal voltage setting of the comparator judgement range and verification of one-bit data accuracy warranty of the gradation output voltage with respect to the input data to the LCD driver.

[0064]

The flowchart in Fig.6 is in common with the flowchart shown in Fig.5 only in the respect of the setting of the reference power supply voltage, and is elaborated as to the set items to be varied for each gradation output voltage level.

[0065]

First, at Step S21, the power supply for driving the LCD driver and the reference power supply according to the aforementioned reference power supply voltage setting technique are activated. Then, selection of an input data pattern program is made. Concerning the aforementioned problem, that is, the limited number of pattern programs that can be set in the semiconductor testing device, in this technique pieces of gradation level data to be tested are serially joined one to the next and the start address and stop address of the implementation data for every gradation level are set up so as to produce an integrated input data pattern program.

[0066]

Next, the judgement range required for comparator

judgement is set. This provides the setting of the upper limit level and lower limit level for the gradation output voltage to be tested, whereby the test is effected so that each gradation output voltage level will fall in the range therebetween. Here, the method of setting the voltage values of the upper limit level and lower limit level is the same as the above example.

[0067]

Next, the operation moves to Step S22 in the test flow. Here, to sequentially test all the gradation output voltage levels included between the reference power supply terminals to be tested, level by level, the test gradation number, the expected gradation output voltage level, and the start address and stop address of the input gradation data, are all set up with variables.

The setting of the expected gradation output voltage includes the gradation output voltage level of the relevant test gradation calculated from the reference power supply voltage setting values (calculated by the formula for the ideal value of the gradation output voltage in the LCD driver specification), and the upper limit value and lower limit value calculated from the determined comparator judgement range. The expected output level is loaded for each gradation output voltage level, at the same time, the upper and lower limits for the comparator judgement range, designated at Step

S21, are adapted to be automatically set. At the final step, or Step S23, the data pattern program set beforehand is implemented so as to enable judgement.

[0068]

If this judgement results in FAIL, the test ends immediately. If the judgement results in PASS, the operation returns to Step S22, and the test for the next gradation output voltage level is carried out, and the same test is repeated until all the gradation output voltage levels included between the reference power supply voltage terminals set as the test target are completed.

[0069]

As has been described heretofore, the mutual relationship between the input gradation level data, the expected output voltage level (judgement level of the comparison judgement circuit) and the temporal setting of the test gradation number is made coincident within each test gradation level unit. Here, the test for every gradation level is sequentially repeated up to the designated gradation level. If all the gradation output voltage levels to be test result in PASS, the operation moves to the test for the gradation levels corresponding to the settings of the next reference power supply. If the test results in FAIL for some gradation level in the process, the test is ended at that point. Compared to the testing method using high-accuracy voltmeters whereby

gradation output voltage measurement data for all gradations and all outputs should be temporarily stored in memory so as to make judgement based on computational processing, it is also effective in reducing the testing time for an identical defective device.

[0070]

Turning to another matter, the fail check technique devised as a means for easy verification of one-bit accuracy warranty will be described. The fail check described herein is to verify that, if an output voltage other than the expected value for the predetermined gradation input data is output due to defective input of the input data, etc., this can be positively discriminated as an imperfection. For example, bit accuracy can be assured by confirming that a product with one-bit shift failure of the input data (failure of the output gradation voltage shifting by one gradation level) will never be selected as a non-defective product as a result of the fact that the comparator judgement range is too large.

[0071]

As stated above, the mutual relationship between the input gradation data and the expected output voltage level (judgement level based on the comparison judgement circuit) and the temporal change of the setting of the test gradation number always agree for each gradation level to be tested. Accordingly, when the N-th gradation level is tested, the

gradation data input and expected output voltage corresponding to the N-th gradation are set. Fail check is carried out by changing the expected output voltage for testing the N-th gradation level to that for the (N+1)-th gradation level and to that for the (N-1)-th gradation level and confirming that all the tests fail for all the gradation levels. As stated above, since the expected output voltage is set as a variable, it can be executed by a simple change of the program. The same effect can be obtained by changing the address of the gradation input data by one gradation. Since the expected values for the (N+1)-th gradation level and the (N-1)-th gradation level represent the least significant bit of the input data, the test program implemented by this fail check technique can realize one-bit accuracy warranty.

[0072]

[Effect of the Invention]

As detailed above, according to the present invention, the assurance of high test accuracy in the gradation output voltage test and reduction of the testing time can be realized simultaneously.

For the test time by high-accuracy voltmeter, the outputs of the gradation output voltages from the LCD driver are serially measured, one by one, for each gradation level. In contrast, in comparator judgement, all the outputs of the gradation output voltages from the LCD driver are tested in

parallel simultaneously. Therefore, if the testing time is calculated for the 480 outputs of an LCD driver model of 256 gradation levels assuming the gradation output voltage drive time (including output delay time) of this LCD driver to be 20 [μS], the voltage measurement time by the high-accuracy voltmeter results in 480 × 256 × 20 = 2457.6 [mS].

[0073]

Here, this value shows the voltmeter measurement time. As to the actual total testing time, the memory storage time for each voltage data and computation processing time have to be further added.

As to the testing time due to comparator judgement, since all outputs can be judged together simultaneously, the testing time is calculated to be

1 × 256 × 20 = 5.12 [mS]. Hence, compared to the testing time with the conventional high-accuracy voltmeter, the testing time is reduced by 1/480 (one over the number of output terminals of the LCD driver).

[0074]

Moreover, the present invention does not require additional special testing circuits to the conventional inexpensive semiconductor testing device, can also handle the test for the future LCD drivers with multi-output and multi-gradation, can greatly contribute to reduction in testing cost, and can also realize use of existing equipment.

[BRIEF DESCRIPTION OF THE DRAWINGS]

[Fig.1]

Fig.1 is a circuit block diagram of one embodiment of the present invention showing the settings of applying reference power supply voltages for an LCD driver LSI with a reference power supply generating circuit of a Gamma correction resistance type.

[Fig.2]

Fig.2 is a waveform chart showing gradation output voltage, for explanation of the operation of the same embodiment.

[Fig.3]

Fig.3 is a circuit block diagram of another embodiment of the present invention showing the settings of applying reference power supply voltages for an LCD driver LSI with a reference power supply generating circuit of a Gamma correction resistance type.

[Fig.4]

Fig.4 is a circuit block diagram of another embodiment of the present invention showing the settings of applying reference power supply voltages for an LCD driver LSI with a reference power supply generating circuit of a Gamma correction resistance type.

[Fig.5]

Fig.5 is a test flowchart for conventional comparator

judgement.

[Fig.6]

Fig.6 is a test flowchart according to the embodiment of the present invention.

[Fig.7]

Fig.7 is a constructional diagram showing a block structure for high-accuracy voltage meter judgement of a conventional LCD driver LSI testing device.

[Fig.8]

Fig.8 is a constructional diagram showing a block structure for comparator judgement of a conventional LCD driver LSI testing device.

[Fig.9]

Fig.9 is a waveform chart of gradation output voltages for explanation of the operation when application of conventional reference power supply voltages is set.

[Fig.10]

Fig.10 is a circuit block diagram showing an LCD driver disclosed in Japanese Patent Application Laid-open 2000-165244.

[Fig.11]

Fig.11 is a circuit block diagram showing the setting of applying conventional reference power supply voltages.

[DESCRIPTION OF REFERENCE NUMERALS]

1 LCD driver LSI

2-1, 2-2, ···2-m DA converters

3-1, 3-2, ···3-m output terminals from the LCD driver

4 data memory

5 high-accuracy analog voltmeter

6-1, 6-2, ···6-x reference power supply voltage input terminals to the LCD driver

7 tester power supply

8 reference voltage generating circuit of an LCD driver

9 Computational Device

10 semiconductor testing device, tester

11-1, 11-2, ···11-m tester channels

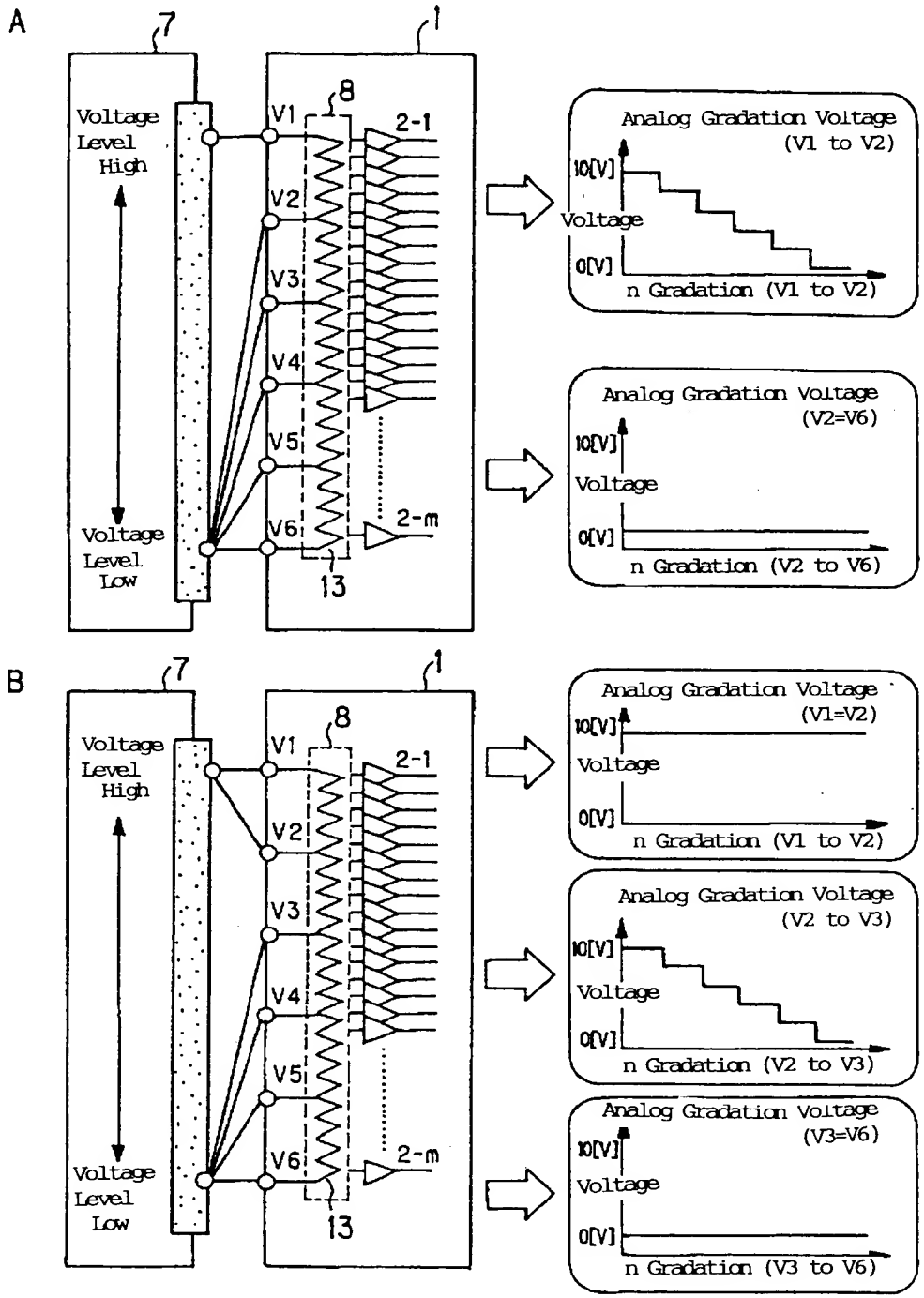
12-1, 12-2, ···12-m comparators

13 Gamma correction resistance

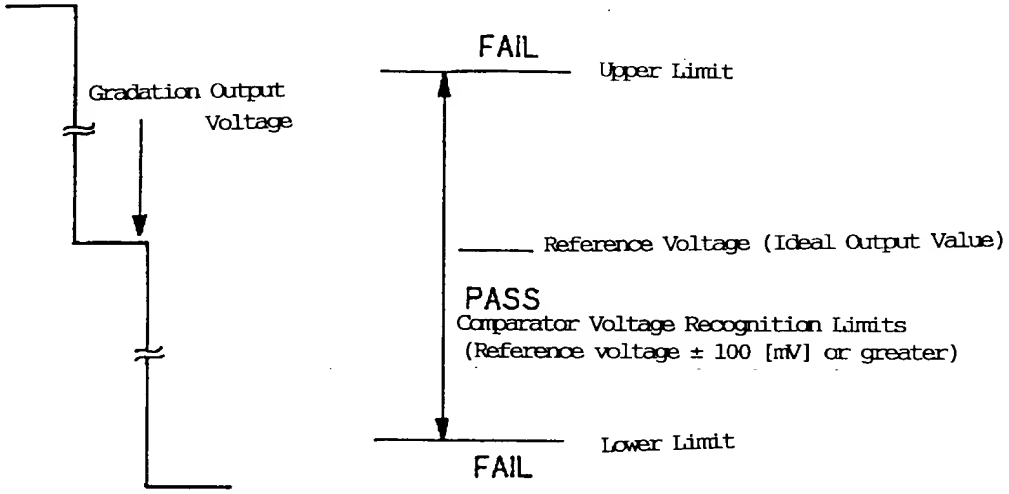
V1, V2, ··· V6 reference power supply voltage input terminals to the LCD driver

[NAME OF DOCUMENT] DRAWINGS

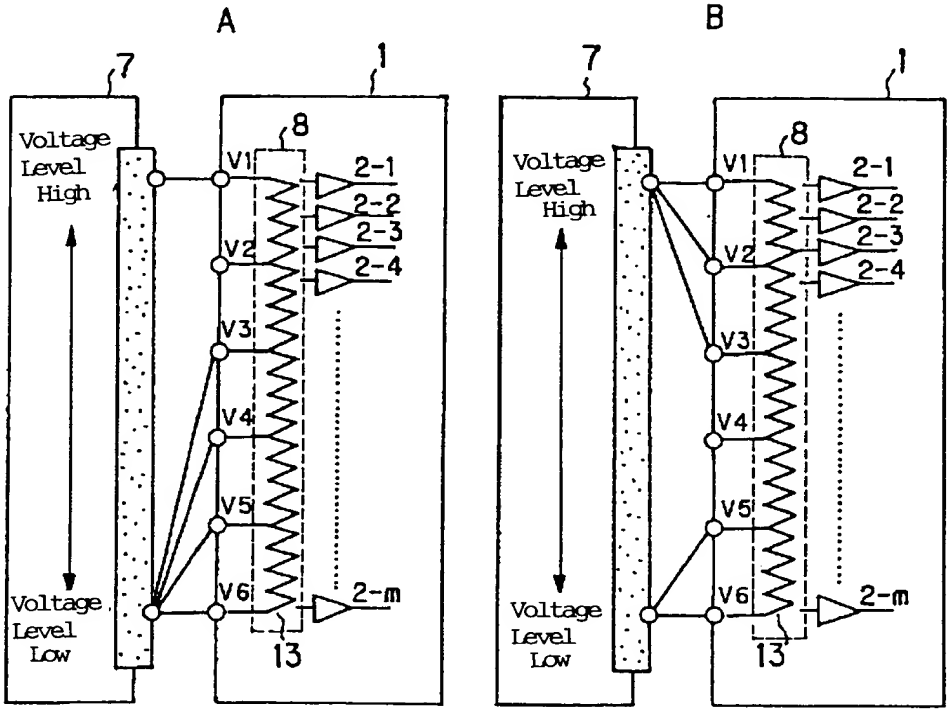
[FIG.1]



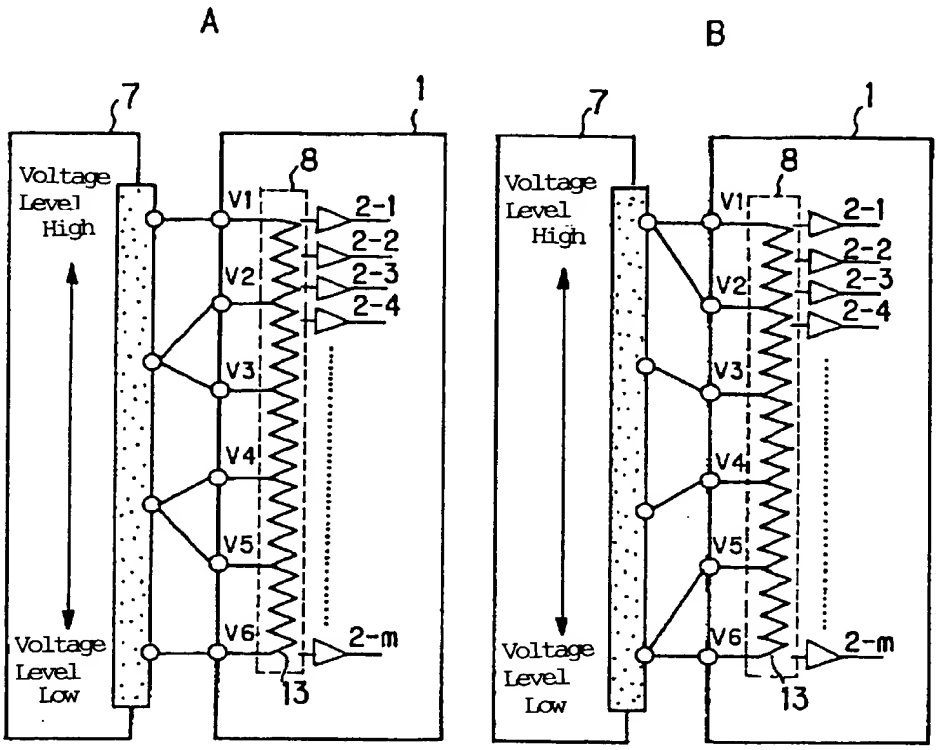
[FIG.2]


Gradation Output Voltage
FAIL
Upper Limit
Reference Voltage (Ideal Output Value)
PASS
Comparator Voltage Recognition Limits
(Reference voltage ± 100 [mV] or greater)
Lower Limit
FAIL

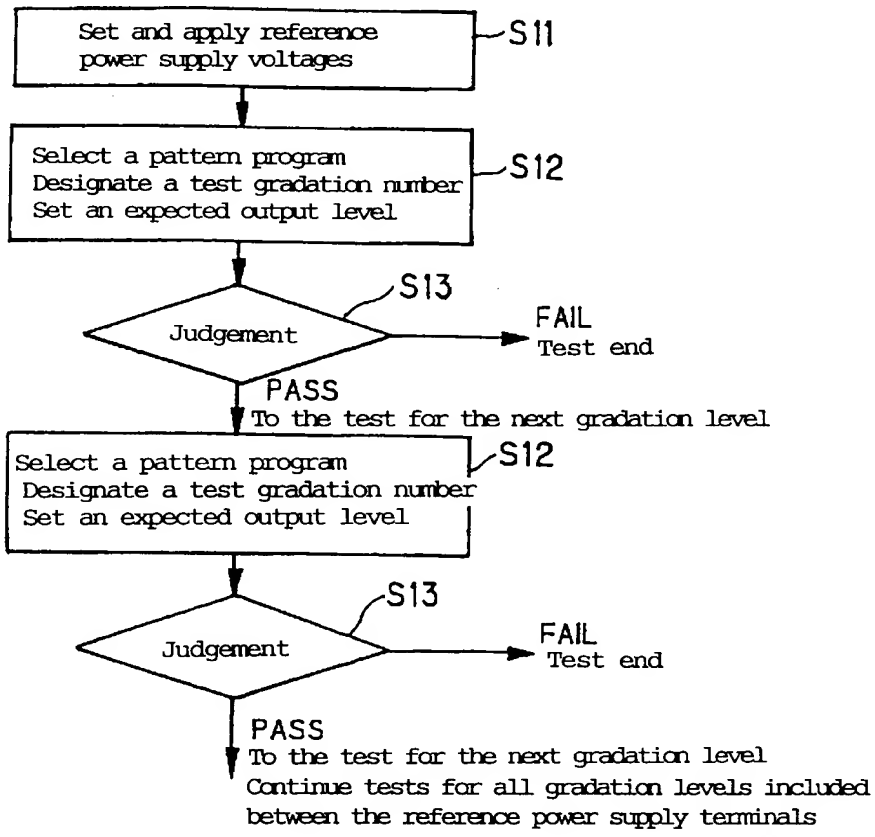
[FIG.3]


A
B
7
1
8
Voltage Level High
Voltage Level Low
V1
V2
V3
V4
V5
V6
2-1
2-2
2-3
2-4
2-m
13

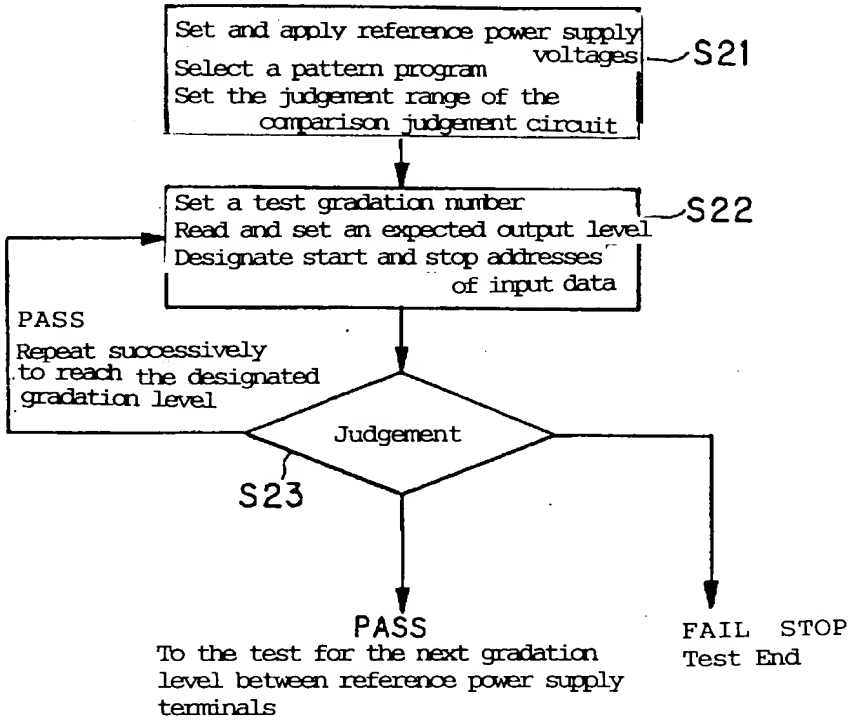
[FIG.4]


A
B
7
1
8
Voltage Level High
Voltage Level Low
V1
V2
V3
V4
V5
V6
2-1
2-2
2-3
2-4
2-m
13

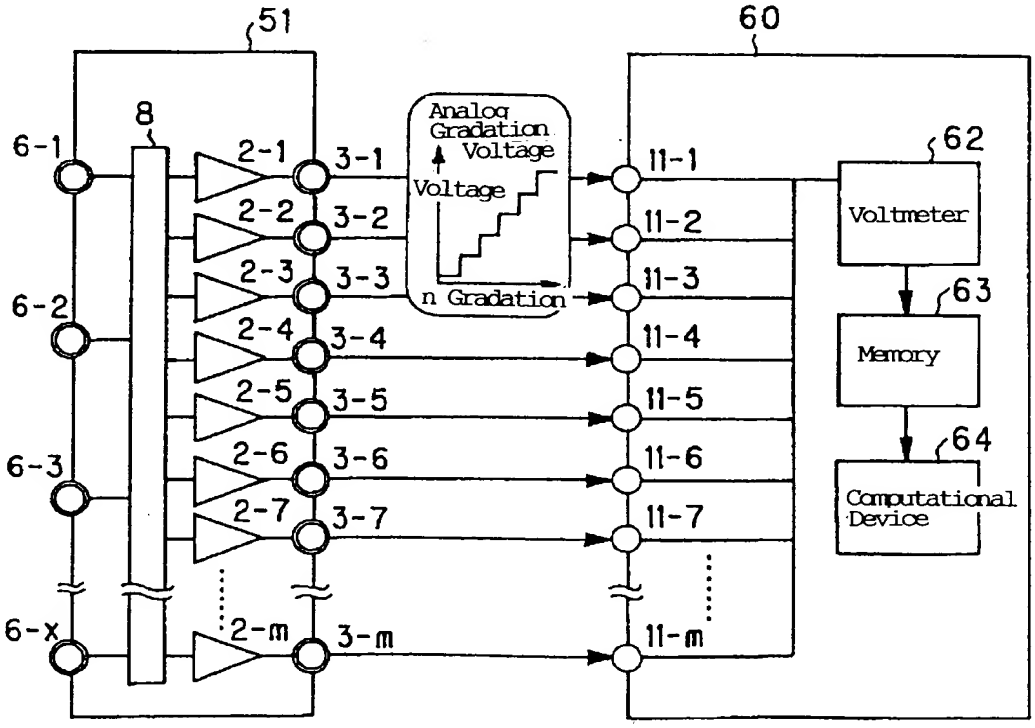
[FIG.5]


Set and apply reference power supply voltages
S11
Select a pattern program
Designate a test gradation number
Set an expected output level
S12
Judgement
S13
FAIL
Test end
PASS
To the test for the next gradation level
Select a pattern program
Designate a test gradation number
Set an expected output level
S12
Judgement
S13
FAIL
Test end
PASS
To the test for the next gradation level
Continue tests for all gradation levels included between the reference power supply terminals

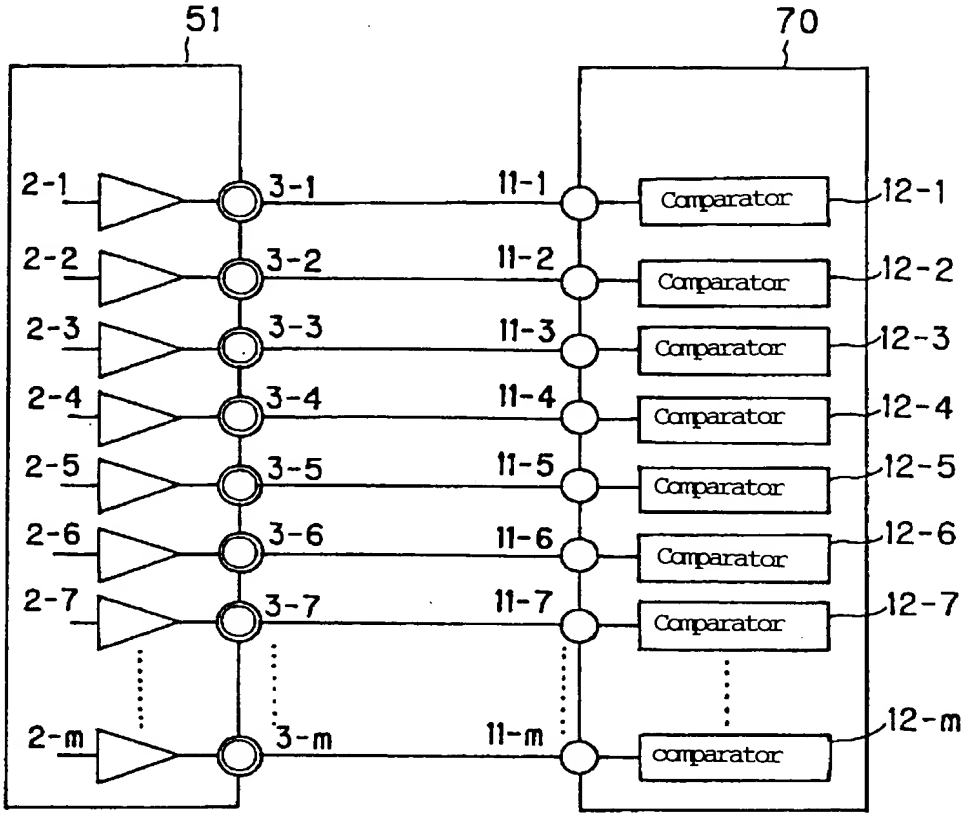
[FIG.6]


Set and apply reference power supply voltages
Select a pattern program
Set the judgement range of the comparison judgement circuit
S21
Set a test gradation number
Read and set an expected output level
Designate start and stop addresses of input data
S22
PASS
Repeat successively to reach the designated gradation level
Judgement
S23
PASS
To the test for the next gradation level between reference power supply terminals
FAIL STOP
Test End

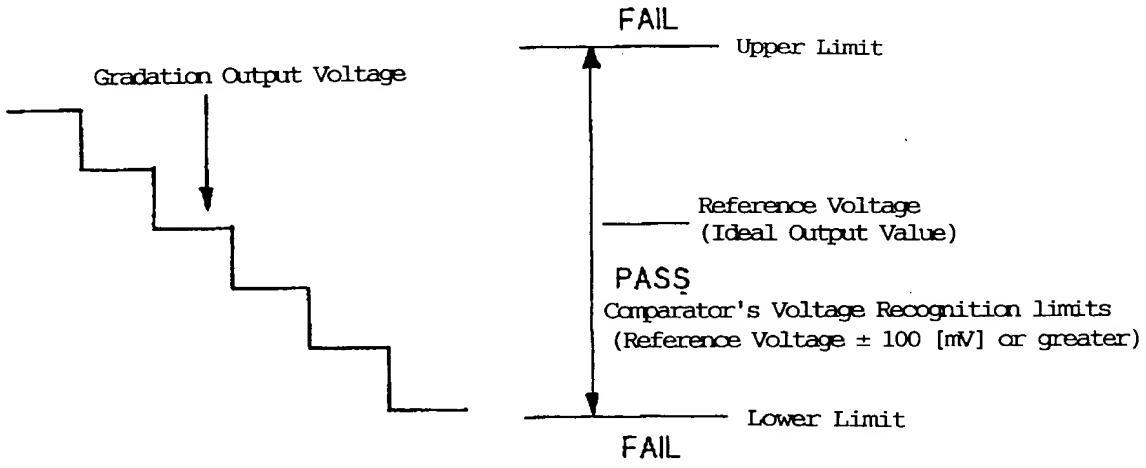
[FIG.7]


51
60
8
6-1
6-2
6-3
6-x
2-1
2-2
2-3
2-4
2-5
2-6
2-7
2-m
3-1
3-2
3-3
3-4
3-5
3-6
3-7
3-m
Analog Gradation Voltage
Voltage
n Gradation
11-1
11-2
11-3
11-4
11-5
11-6
11-7
11-m
62
Voltmeter
63
Memory
64
Computational Device

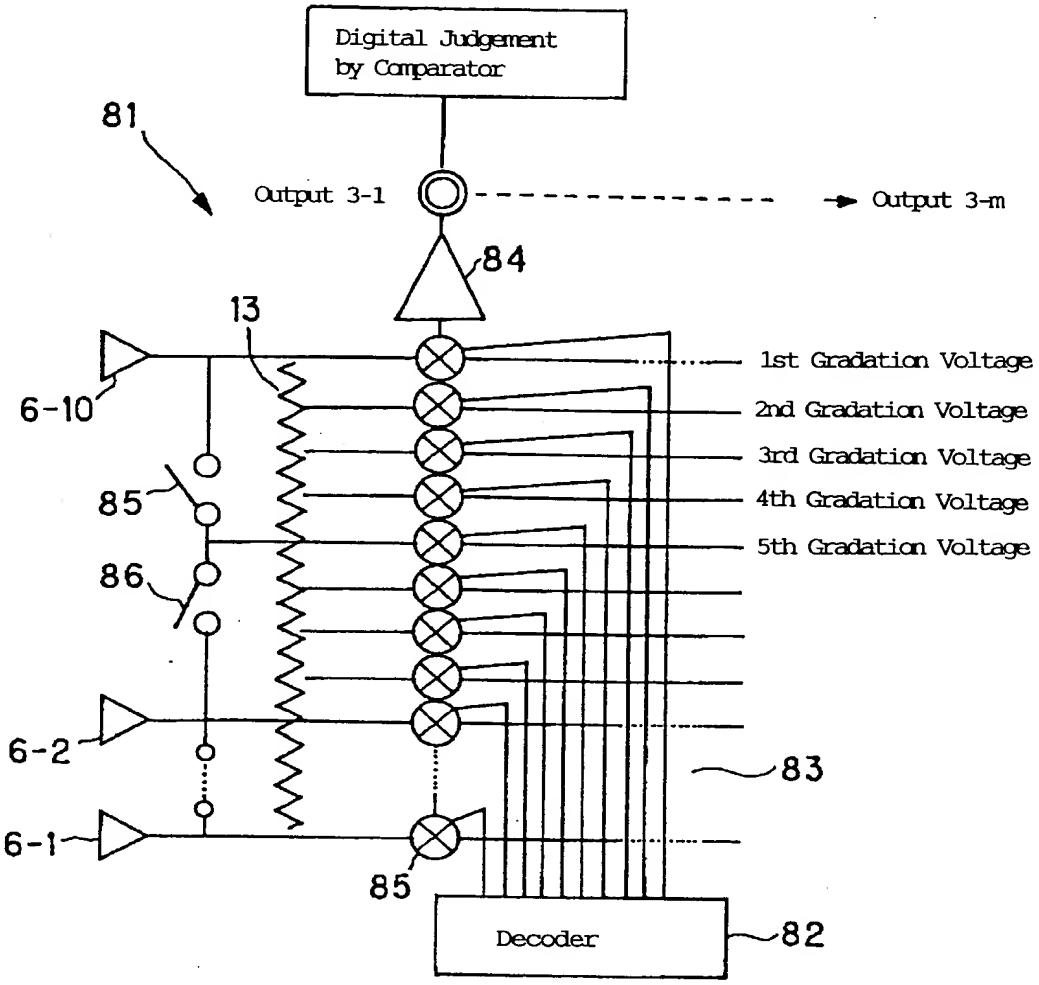
[FIG.8]


51
70
2-1
3-1
11-1
Comparator
12-1
2-2
3-2
11-2
Comparator
12-2
2-3
3-3
11-3
Comparator
12-3
2-4
3-4
11-4
Comparator
12-4
2-5
3-5
11-5
Comparator
12-5
2-6
3-6
11-6
Comparator
12-6
2-7
3-7
11-7
Comparator
12-7
2-m
3-m
11-m
comparator
12-m

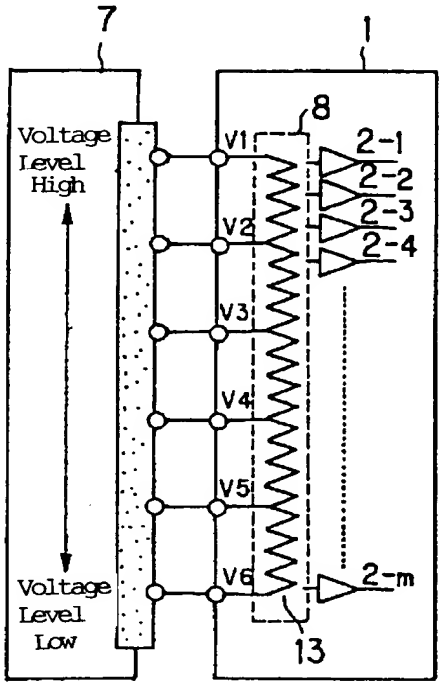
[FIG.9]


FAIL
Upper Limit
Gradation Output Voltage
Reference Voltage
(Ideal Output Value)
PASS
Comparator's Voltage Recognition limits
(Reference Voltage ± 100 [mV] or greater)
Lower Limit
FAIL

[FIG.10]


Digital Judgement by Comparator
81
Output 3-1
Output 3-m
84
13
6-10
85
86
6-2
6-1
85
1st Gradation Voltage
2nd Gradation Voltage
3rd Gradation Voltage
4th Gradation Voltage
5th Gradation Voltage
83
Decoder
82

[FIG.11]


7
1
8
Voltage Level High
Voltage Level Low
V1
V2
V3
V4
V5
V6
2-1
2-2
2-3
2-4
2-m
13

[NAME OF DOCUMENT] ABSTRACT

[ABSTRACT]

[OBJECT]

The object is to provide a testing method for semiconductor integrated circuits and a testing device therefor, which realizes sharp reduction in testing time and high-accuracy testing regardless of the measurement accuracy of the judgement module.

[MEANS FOR SOLUTION]

The set values of reference power supply voltages are assigned at 10 [V] and 0 [V], the upper limit and lower limit of the drive voltage specification of an LCD driver. A reference power supply potential difference of 10 [V] is created between reference power supply terminals V1 and V2. Testing the gradation levels included between the reference power supply terminals V1 and V2 makes it possible to create a potential difference of about 200 [mV] (potential difference between the reference power supply terminals, 10000 [mV]/51 gradation levels) between adjacent output gradation levels. The gradation levels included between the reference power supply terminals are tested while the input data and the setting of the comparator judgement range are sequentially switched for every gradation level, thus all the gradation levels included in that section are tested.

[SELECTED DRAWING] FIG.1

Information of Applicant Data

Identification No. [000005049]

1. Change Date August 29, 1990

[Reason of Change] New register

Residence 22-22, Nagaike-cho, Abeno-ku, Osaka-shi, Osaka

Name SHARP KABUSHIKI KAISHA